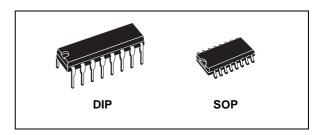


# MICROPOWER PHASE-LOCKED LOOP

- QUIESCENT CURRENT SPECIFIED UP TO 20V
- VERY LOW POWER CONSUMPTION: 70μW
   (TYP.) AT VCO f<sub>0</sub> = 10kHz, V<sub>DD</sub> = 5V
- OPERATING FREQUENCY RANGE: UP TO 1.4MHz (TYP.) AT V<sub>DD</sub> = 10V
- LOW FREQUENCY DRIFT : 0.04%/°C (typ.) AT V<sub>DD</sub> = 10V
- CHOICE OF TWO PHASE COMPARATORS:
   1) EXCLUSIVE OR NETWORK
   2) EDGE-CONTROLLED MEMORY
   NETWORK WITH PHASE-PULSE OUTPUT
   FOR LOCK INDICATION
- HIGH VCO LINEARITY: <1% (TYP.)
- VCO INHIBIT CONTROL FOR ON-OFF KEYING AND ULTRA-LOW STANDBY POWER CONSUMPTION
- SOURCE-FOLLOWER OUTPUT OF VCO CONTROL INPUT (demod. output)
- ZENER DIODE TO ASSIST SUPPLY REGULATION
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I<sub>I</sub> = 100nA (MAX) AT V<sub>DD</sub> = 18V T<sub>A</sub> = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



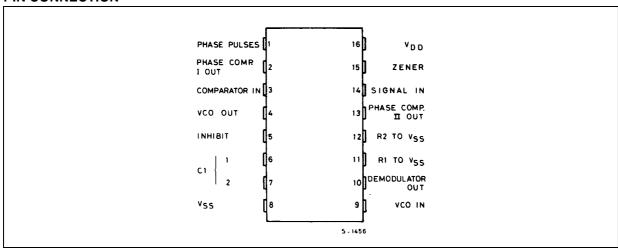
#### **ORDER CODES**

PACKAGE	TUBE	T & R
DIP	HCF4046BEY	
SOP	HCF4046BM1	HCF4046M013TR

#### **DESCRIPTION**

The HCF4046B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor Technology, available in 16-lead dual in-line plastic or ceramic package. The HCF4046B CMOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2V zener diode is provided for supply regulation if necessary.

### **PIN CONNECTION**



September 2001 1/12

#### **VCO Section**

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance  $(10^{12}\Omega)$  of the VCO simplifiers the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R  $_{S})$  of 10  $K\Omega$  or more should be connected from this terminal to  $V_{\mbox{\scriptsize SS}}$ . If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the HCF4024B, HCF4018B, HCF4020B, HCF4022B, HCF4029B and HBF4059A. One or more HCF4018B (Presettable Divide-by-N Counter) or HCF4029B (Presettable Up/Down Counter), or HBF4059A (Programmable Divide-by-"N" Counter), together with HCF4046B the (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

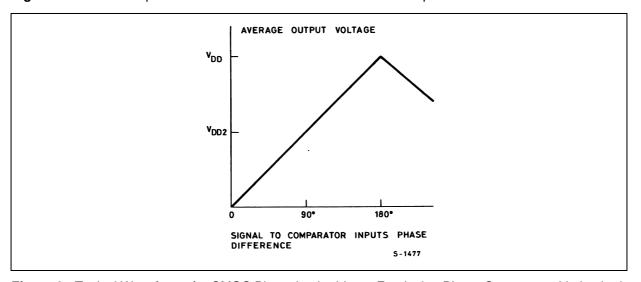
### **Phase Comparators**

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" ≤ 30% of  $(V_{DD}-V_{SS})$ , logic "1"  $\geq 70\%$  of  $(V_{DD}-V_{SS})$ ]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input. Phase comparator I is an exclusive-OR network; it operates analogously to an over-driven balanced mixer. To maximize the lock range, the signal-and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to V<sub>DD</sub>/2. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (fo). The frequency range of

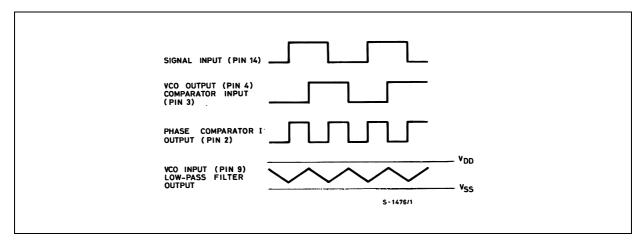
input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range (2 f<sub>C</sub>). The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range (2  $f_1$ ). The capture range is  $\leq$  the lock range. With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal. One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics the VCO center-frequency. A second of characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig.1 shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. **Typical** waveforms for а **CMOS** phase-locked-loop employing phase comparator I in locked condition of fo is shown in fig.2. Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-stage output-circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V<sub>DD</sub> or down to V<sub>SS</sub>, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the

p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the pand n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig.3 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

Figure 1: Phase-Comparator I Characteristics at Low-Pass Filter Output.

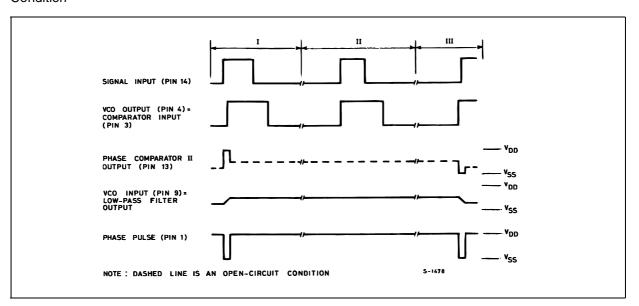


 $\textbf{Figure 2}: \textbf{Typical Waveforms for CMOS Phase Locked-Loop Employing Phase Comparator I in Locked Condition of } f_o$ 

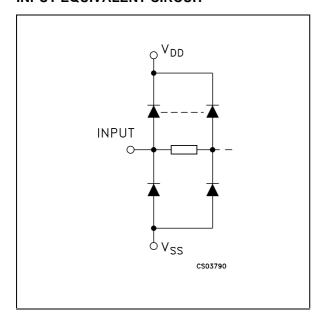


4

**Figure 3 :** Typical Waveforms for CMOS Phase-locked Loop Employing Phase Comparator II In Locked Condition



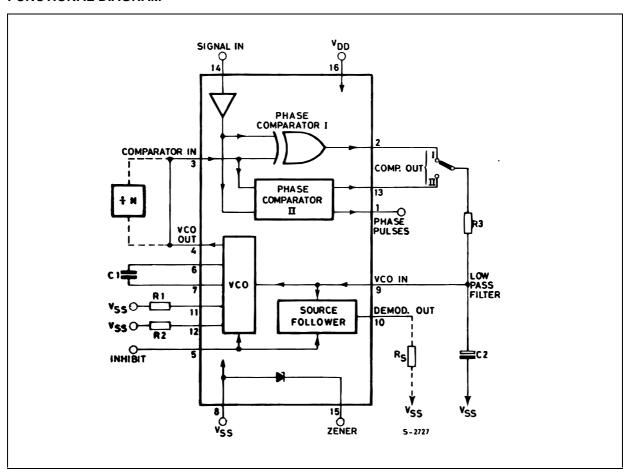
## **INPUT EQUIVALENT CIRCUIT**



## **PIN DESCRIPTION**

PIN No	SYMBOL	NAME AND FUNCTION
1	PHASE PULSES	Phase Comparator Pulse Output
2	PHASE COMP I OUT	Phase Comparator 1 Output
3	COMPARATOR IN	Comparator Input
4	VCO OUT	VCO Output
5	INHIBIT	Inhibit Input
6, 7	C1	Capacitors
9	VCO IN	VCO Input
10	DEMODULATOR OUT	Demodulator Output
11	R <sub>1</sub> TO V <sub>SS</sub>	Resistor R1 Connection
12	R <sub>2</sub> TO V <sub>SS</sub>	Resistor R2Connection
13	PHASE COMP II OUT	Phase Comparator 2 Output
14	SIGNAL IN	Signal Input
15	ZENER	Diode Zener
8	V <sub>SS</sub>	Negative Supply Voltage
16	$V_{DD}$	Positive Supply Voltage

## **FUNCTIONAL DIAGRAM**



## **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
V <sub>I</sub>	DC Input Voltage	-0.5 to V <sub>DD</sub> + 0.5	V
l <sub>l</sub>	DC Input Current	± 10	mA
P <sub>D</sub>	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T <sub>op</sub>	Operating Temperature	-55 to +125	°C
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V<sub>SS</sub> pin voltage.

## **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
V <sub>I</sub>	Input Voltage	0 to V <sub>DD</sub>	V
T <sub>op</sub>	Operating Temperature	-55 to 125	°C



# DC SPECIFICATIONS

		Test Condition			Value								
Symbol	Parameter	V <sub>I</sub>	v <sub>o</sub>	lo	V <sub>DD</sub>	T <sub>A</sub> = 25°C		-40 to 85°C		-55 to	125°C	Unit	
		(V)	(V)	(μ <b>A</b> )	(V)	Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
VCO SE	CTION			•	•								
V <sub>OH</sub>	High Level Output	0/5		<1	5	4.95			4.95		4.95		
	Voltage	0/10		<1	10	9.95			9.95		9.95		V
		0/15		<1	15	14.95			14.95		14.95		
$V_{OL}$	Low Level Output	5/0		<1	5		0.05			0.05		0.05	
	Voltage	10/0		<1	10		0.05			0.05		0.05	V
		15/0		<1	15		0.05			0.05		0.05	
I <sub>OH</sub>	Output Drive	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		
	Current	0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		mA
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		IIIA
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I <sub>OL</sub>	Output Sink	0/5	0.4	<1	5	0.44	1		0.36		0.36		
	Current	0/10	0.5	<1	10	1.1	2.6		0.9		0.9		mΑ
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
l <sub>l</sub>	Input Leakage Current	0/18	Any In	put	18		±10 <sup>-5</sup>	±0.1		±1		±1	μΑ
PHASE (	OMPARATOR SEC	TION	I.			I	I	I	I	I	ı	l	
I <sub>DD</sub>	Total Device	0/5			5		0.05	0.1		0.1		0.1	
	Current	0/10			10		0.25	0.5		0.5		0.5	mA
	Pin 14= Open	0/15			15		0.75	1.5		1.5		1.5	
	Pin 5= V <sub>DD</sub>	0/20			20		2	4		4		4	
	Total Device	0/5			5		0.04	5		150		150	
	Current	0/10			10		0.04	10		300		300	
	Pin 14= V <sub>SS</sub> or V <sub>DD</sub>	0/15			15		0.04	20		600		600	μΑ
	Pin 5= V <sub>DD</sub>	0/20			20		0.08	100		3000			
I <sub>OH</sub>	Output Drive	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		
0	Current	0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		4
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		mA
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I <sub>OL</sub>	Output Sink	0/5	0.4	<1	5	0.44	1		0.36		0.36		
02	Current	0/10	0.5	<1	10	1.1	2.6		0.9		0.9		mΑ
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
V <sub>IH</sub>	High Level Input		0.5/4.5	<1	5	3.5			3.5		3.5		
	Voltage		1/9	<1	10	7			7		7		V
			1.5/13.5	<1	15	11			11		11		
V <sub>IL</sub>	Low Level Input		4.5/0.5	<1	5			1.5		1.5		1.5	
	Voltage		9/1	<1	10			3		3		3	V
			13.5/1.5	<1	15			4		4		4	
I <sub>I</sub>	Input Leakage Current	0/18	Any In	put	18		±10 <sup>-5</sup>	±0.1		±1		±1	μΑ
l <sub>OUT</sub>	High Impedance Leakage Current	0/18	Any In	put	18		±10 <sup>-4</sup>	±0.4		±12		±12	μΑ
C <sub>I</sub>	Input Capacitance		Any In	put			5	7.5					pF
	Margin for both "1" and "0	<u> </u>	_	-		<u> </u>			<u> </u>	<u> </u>	<u> </u>		יץ

The Noise Margin for both "1" and "0" level is: 1V min. with  $V_{DD}$ =5V, 2V min. with  $V_{DD}$ =10V, 2.5V min. with  $V_{DD}$ =15V

# **ELECTRICAL CHARACTERISTICS** $(T_{amb} = 25^{\circ}C)$

Cumele el	Deverantes		'					
Symbol	Parameter	V <sub>DD</sub> (V)			Min.	Тур.	Max.	Unit
VCO SEC	TION		•		•			
$P_{D}$	Operating Power	5	f <sub>O</sub> = 10KHz	$R1 = 10M\Omega$		70	140	
	Dissipation	10	R2 = ∞	$V_{COIN} = V_{DD}/2$		800	1600	μW
		15				3000	6000	
$f_{MAX}$	Maximum	5	$R_1 = 10K\Omega$	C1 = 50pF	0.3	0.6		
	frequency	10	R2 = ∞	$V_{COIN} = V_{DD}$	0.6	1.2		ns
		15			8.0	1.6		
		5	$R_1 = 5K\Omega$	C1 = 50pF	0.5	8.0		
		10	R2 = ∞	$V_{COIN} = V_{DD}$	1	1.4		ns
		15			1.4	2.4		
	Center Frequency (f <sub>O</sub> ) and frequency	I		ernal components R <sub>1</sub> , Design Information	R <sub>2</sub> , and	C <sub>1</sub>		
	Range f <sub>max</sub> - f <sub>min</sub> Linearity	5	$V_{COIN} = 2.5V^{\pm 0.3}$	$R_1 = 10K\Omega$	1	1.7		
		10	$V_{COIN} = 2.5V$ $V_{COIN} = 5V^{\pm 1}$	$R_1 = 10000$ $R_1 = 10000$	+	0.5		
		10	$V_{COIN} = 5V$ $V_{COIN} = 5V^{\pm 2.5}$	$R_1 = 100K\Omega$ $R_1 = 400K\Omega$	+	4		%
		15	$V_{\text{COIN}} = 7.5 V^{\pm 1.5}$	$R_1 = 100K\Omega$		0.5		70
		15	$V_{COIN} = 7.5V^{\pm 5}$	$R_1 = 100R_2$ $R_1 = 1M\Omega$		7		
	Temperature	5	VCOIN =1.5V	177 - 110122		±0.12		
	Frequency Stability	10				±0.12		
	(no frequency offset) f <sub>min</sub> = 0							
		15				±0.015		%/°C
	Temperature	5				±0.09		70, 0
	Frequency Stability (frequency offset)	10				±0.07		
	$f_{min} = 0$	15				±0.03		
VCO	Output Duty Cycle	5, 10, 15				50		%
t <sub>TLH</sub> t <sub>THL</sub>	VCO Output	5				100	200	
	Transition Time	10				50	100	ns
		15				40	80	
put ( Outp	Source Follower Output (Demodulated Output): Offset Voltage V <sub>COIN</sub> -V <sub>DEM</sub>	5, 10, 15	R <sub>S</sub> > 10KΩ			1.8	2.5	V
	Source Follower Output (Demodulated	5	$R_S = 100 K\Omega$	$V_{COIN} = 2.5 V^{\pm 0.3}$		0.3		
	Output): Linearity	10	R <sub>S</sub> = 300KΩ	$V_{COIN} = 5V^{\pm 2.5}$		0.7		%
		15	R <sub>S</sub> = 500KΩ	$V_{COIN} = 7.5V^{\pm 5}$		0.9		
V <sub>Z</sub>	Zener Diode Voltage		I <sub>Z</sub> = 50 μA		4.45	5.5	7.5	V
$R_Z$	Zener Dynamic Resistance		$I_Z = 1 \text{ mA}$			40		Ω

	Damana da	Test Condition		\	Value (*)		
Symbol	Parameter	V <sub>DD</sub> (V)		Min.	Тур.	Max.	Uni
PHASE C	OMPARATOR SECTI	ON		<u>'</u>	I	ı	ı
R14	Pin 14 (signal in)	5		1	2		
	Input Resistance	10		0.2	0.4		$M\Omega$
		15		0.1	0.2		
	AC Coupled Signal	5	f <sub>IN</sub> = 100KHz sine wave		180	360	
	Input Sensivity (*)	10			330	660	m۷
	(peak to peak)	15			900	1800	
t <sub>PLH</sub>	Propagation Delay	5			225	450	
	Time High to Low	10			100	200	ns
	Level Pins 14 to 1	15			65	130	
t <sub>PLH</sub>	Propagation Delay	5			350	700	
	Time Low to High Level	10			150	300	ns
		15			100	200	
t <sub>PHZ</sub>	Disable Time High	5			225	450	
	Level to High	10			100	200	ns
	Impedance Pins 14 to 13	15			65	130	
t <sub>PLZ</sub>	Disable Time Low	5			285	570	
	Level to High	10			130	260	ns
	Impedance	15			95	190	
t <sub>r</sub> t <sub>f</sub>	Input Rise or Fall	5				50	
	Time Comparator	10				1	μs
	Pin 3	15				0.3	
	Signal Pin 14	5				500	
		10				20	μs
		15				2.5	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time	5			100	200	
		10			50	100	ns
		15	n 10KHz for Phase Comparator II		40	80	

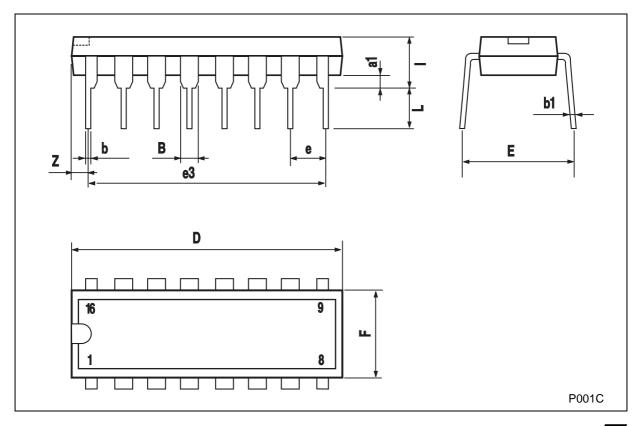
**DESIGN INFORMATION** This information is a guide for approximating the value of external components in a Phase-Locked-Loop system. The selected external components must be within the following ranges:  $5K\Omega \leq R_1,\ R_2,\ R_S \leq 1M\Omega \qquad C_1 \geq 100 pF \ at \ V_{DD} \geq 5V \qquad C_1 \geq 50 pF \ at \ V_{DD} \geq 10V$ 

	USING PHASE (	COMPARATOR I	USING PHASE (	COMPARATOR II	
CHARACTERISTICS	VCO WITHOUT OFFSET R2=∞	VCO WITH OFFSET	VCO WITHOUT OFFSET R2=∞	VCO WITH OFFSET	
VCO Frequency	to to INPUT VOLTAGE 5-1479	t <sub>max</sub> to to to to to VCO INPUT VOLTAGE 5-1480	10 21L 10 YDD2 YDD VCO INPUT VOLTAGE 5-1478	10 121L VOO2 VOO	
For No Signal Input	VCO in PLL System Freque	ency f <sub>o</sub>	Operating F	will Adjust to Lowest requency fo	
Frequency Lock Range, 2f <sub>L</sub>		<del>-</del>	Frequency Range f <sub>max</sub> - f <sub>min</sub>		
Frequency Lock Range, 2f <sub>C</sub>	R3 IN ○ R3 Y1 = R3 C2 C2	O OUT $(1),(2)$ $2^{\dagger}_{C} \approx \frac{1}{\pi} \sqrt{\frac{2\pi t_{L}}{r_{L}}}$ 5-1483	$f_C = f_1$		
Loop filter Component Section	INO R3	FOR 21 <sub>C</sub> SEE REF. (2)	Ç E		
Phase Angle Between SIgnal and Comparator	90° at Centre frequency (f <sub>O</sub> ), approximating 0° and 180° at ends of lock range (2 f <sub>L</sub> )  Always 0° in lock			0° in lock	
Locks on Harmonics of Centre Frequency	Ye	es	No		
Signal Input Nose Rejection	Hi	gh	Lo	OW	

For further information, see (1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966 (2) G.S. Mosckytz "miniaturized RC filters using phase Lockedloop" BSTJ May 1965

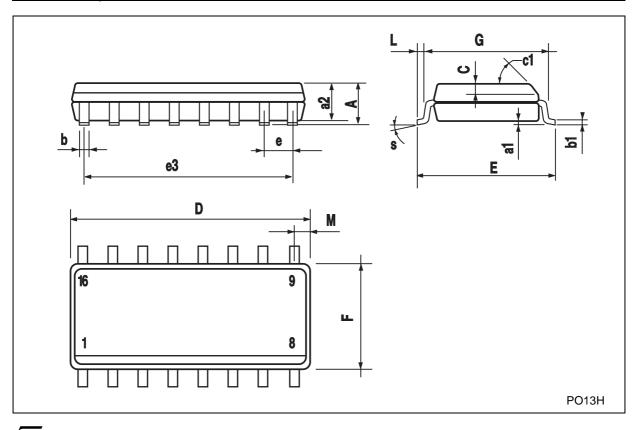
# Plastic DIP-16 (0.25) MECHANICAL DATA

DIM		mm.		inch				
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.		
a1	0.51			0.020				
В	0.77		1.65	0.030		0.065		
b		0.5			0.020			
b1		0.25			0.010			
D			20			0.787		
Е		8.5			0.335			
е		2.54			0.100			
e3		17.78			0.700			
F			7.1			0.280		
I			5.1			0.201		
L		3.3			0.130			
Z			1.27			0.050		



# **SO-16 MECHANICAL DATA**

DIM		mm.		inch				
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.		
Α			1.75			0.068		
a1	0.1		0.2	0.003		0.007		
a2			1.65			0.064		
b	0.35		0.46	0.013		0.018		
b1	0.19		0.25	0.007		0.010		
С		0.5			0.019			
c1			45°	(typ.)	•			
D	9.8		10	0.385		0.393		
Е	5.8		6.2	0.228		0.244		
е		1.27			0.050			
e3		8.89			0.350			
F	3.8		4.0	0.149		0.157		
G	4.6		5.3	0.181		0.208		
L	0.5		1.27	0.019		0.050		
М			0.62			0.024		
S			8° (	max.)	•	•		



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco Singapore - Spain - Sweden - Switzerland - United Kingdom © http://www.st.com

